CERTIFICATE

I, Yuko OKANO, residing at 1-35-21-410, Matsubara, Setagaya-Ku, Tokyo, 156-0043 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2003-054012 and certify that the following is a true translation to the best of my knowledge and belief.

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[Name of Document] SPECIFICATION

[Title of the Invention] CURRENT GENERATING CIRCUIT, ELECTRO-OPTICAL APPARATUS, AND ELECTRONIC UNIT

[Claims]

[Claim 1] A current generating circuit comprising:

a first resistor and a second resistor, one end of each of the first resistor and the second resistor being connected to a power supply terminal to which a power supply voltage is supplied, and a resistance of the first resistor and a resistance of the second resistor being different;

a first transistor for allowing a current corresponding to a voltage of the gate of the first transistor to flow between a first terminal and a second terminal of the first transistor, the first terminal being connected to the other end of the first resistor, and the second terminal and the gate being connected with each other; and

a second transistor for allowing a current corresponding to a voltage of the gate of the second transistor to flow between a first terminal and a second terminal of the second transistor, the first terminal being connected to the other end of the second resistor, and the gate of the second transistor being connected to the gate of the first transistor,

wherein the current flowing in the first transistor is converted into the non-linear current flowing in the second

transistor.

[Claim 2] A current generating circuit comprising:

a first resistor and a second resistor, one end of each of the first resistor and the second resistor being connected to a power supply terminal to which a power supply voltage is supplied, a resistance of the first resistor and a resistance of the second resistor being different, and at least one of the first resistor and the second resistor being a variable resistor;

a first transistor for allowing a current corresponding to a voltage of the gate of the first transistor to flow between a first terminal and a second terminal of the first transistor, the first terminal being connected to the other end of the first resistor, and the second terminal and the gate being connected with each other; and

a second transistor for allowing a current corresponding to a voltage of the gate of the second transistor to flow between a first terminal and a second terminal of the second transistor, the first terminal being connected to the other end of the second resistor, and the gate of the second transistor being connected to the gate of the first transistor.

[Claim 3] A current generating circuit according to claim 2, wherein, between the first resistor and the second resistor, only the first resistor is a variable resistor.

[Claim 4] A current generating circuit according to claim 2 or 3, wherein the variable resistor is configured such that a plurality of resistor devices having predetermined resistances are connected in series with each other.

[Claim 5] A current generating circuit according to claim 2 or 3, wherein the variable resistor is configured such that a plurality of resistor devices having predetermined resistances are connected in parallel with each other.

[Claim 6] A current generating circuit, wherein a plurality of the current generating circuits set forth in claim 1 or 2 are dependently connected, and the current flowing in the second transistor of the current generating circuit disposed at the first stage is allowed to flow in the first transistor of the current generating circuit disposed at the second stage.

[Claim 7] A current generating circuit according to claim 1 or 2, further comprising a D/A conversion circuit for converting digital data into a current signal indicating a current corresponding to the digital data and for allowing the current signal to flow in the first transistor.

[Claim 8] An electro-optical apparatus comprising:

pixel circuits disposed at intersections of a plurality of scanning lines and a plurality of data lines;

a scanning-line drive circuit for selecting the scanning lines; and

a data-line drive circuit including the current generating circuit set forth in any one of claims 1 to 7, and supplying the current flowing in the second transistor of the current generating circuit to the data lines,

the pixel circuit disposed at the intersection between one scanning line and one data line comprising:

a capacitor device for storing electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and

an electro-optical device in which a current corresponding to the electrical charge stored in the capacitor device flows when the selection of the scanning line is finished.

[Claim 9] An electro-optical apparatus comprising:

a plurality of types of pixel circuits corresponding to a plurality of primary colors, the pixel circuits corresponding to the same primary color being disposed at intersections of a plurality of scanning lines and a plurality of data lines such that the pixel circuits share the same data line;

a scanning-line drive circuit for selecting the scanning lines; and

a data-line drive circuit including the current generating circuit set forth in claim 3 for each of the

primary colors, and supplying the current flowing in the second transistor of the current generating circuit corresponding to one primary color to the data line corresponding to the primary color,

the pixel circuit disposed at the intersection between one scanning line and one data line comprising:

a capacitor device for storing electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and

an electro-optical device in which a current corresponding to the electrical charge stored in the capacitor device flows when the selection of the scanning line is finished.

[Claim 10] An electro-optical apparatus according to claim 8, further comprising a setting circuit for setting the resistance of the first resistor or the second resistor of the current generating circuit to a desired value.

[Claim 11] An electro-optical apparatus according to claim 9, further comprising a setting circuit for setting the resistance of the first resistor or the second resistor of the current generating circuit for each of the primary colors.

[Claim 12] An electro-optical apparatus according to claim 10 or 11, further comprising a designation circuit for

designating the resistance to be set by the setting circuit.

[Claim 13] An electro-optical apparatus according to claim 8 or 9, further comprising:

a memory for storing digital data defining the grayscale of the electro-optical device;

a control circuit for reading the digital data from the memory; and

a D/A conversion circuit for converting the digital data read by the control circuit into a current signal indicating a current corresponding to the digital data, and for allowing the current signal to flow in the first transistor of the current generating circuit.

[Claim 14] An electro-optical apparatus according to any one of claims 8 to 13, wherein the electro-optical device is an organic electro luminescence device.

[Claim 15] An electronic unit comprising the electro-optical apparatus set forth in any one of claims 8 to 14.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a current generating circuit, an electro-optical apparatus, and an electronic unit that are suitable for use in driving display panels, for example, organic EL (Electronic Luminescence) panels.

[0002]

[Description of the Related Art]

Organic EL panels are attracting attention as next-generation display panels. The reason for this is that organic EL devices used in organic EL panels are self-light-emitting devices as opposed to liquid crystal devices used in liquid crystal panels that merely change the amount by which the liquid crystal devices transmit light. The organic EL panels also exhibit excellent characteristics, for example, a wider viewing angle, a higher contrast, and a faster response speed than those of the liquid crystal panels. Unlike the liquid crystal devices, which are voltage-driven devices, the organic EL devices are so-called "current-driven devices". Accordingly, for driving the organic EL devices, instead of a voltage, a current should be generated in accordance with the grayscale (luminance) level, and thus, a current generating D/A converter has been invented (for example, see Patent Document 1).

[0003]

It is generally known that the humans' visual characteristics have logarithmic or exponential properties. Even if the grayscale changes linearly, it does not sometimes appear to the humans' eyes that the grayscale changes linearly. In view of these circumstances, it is common that non-linear characteristics (γ characteristics), for example, logarithmic or exponential characteristics, are provided in an electro-optical apparatus so that they appear to be linear characteristics for the humans' eyes. This type of processing is sometimes referred to as "γ correction".

The following operation can be considered when taken this γ correction into consideration. A current signal having non-linear characteristics is generated for digital data indicating that the grayscale (luminance) of organic EL devices is linear, and is then provided to the organic EL devices, thereby allowing an observer to visually recognize that the grayscale changes linearly.

As the above type of operation, the following operations, for example, can be considered: (1) digital data having linear characteristics is converted into digital data having non-linear characteristics by using a table; and (2) the grayscale range represented by digital data is divided into a plurality of areas, and in the divided areas,

required γ characteristics are approximated by using a plurality of linear characteristics.

[0004]

[Patent Document 1]

Japanese Unexamined Patent Application Publication No. 2000-122608

[0005]

[Problems to be Solved by the Invention]

However, the operation (1) makes the circuit complicated, and the operation (2) makes it difficult to obtain smooth γ characteristics.

In view of this background, it is an object of the present invention to provide a current generating circuit having a simple circuit configuration and obtaining smooth, non-linear characteristics (γ characteristics), and also to provide an electro-optical apparatus and an electronic unit using such a current generating circuit.

[0006]

[Means for Solving the Problems]

In order to achieve the above object, a current generating circuit of the present invention includes: a first resistor and a second resistor, one end of each of the first resistor and the second resistor being connected to a power supply terminal to which a power supply voltage is supplied, and the resistance of the first resistor and the

resistance of the second resistor being different; a first transistor for allowing a current corresponding to the voltage of the gate of the first transistor to flow between a first terminal and a second terminal of the first transistor, the first terminal being connected to the other end of the first resistor, and the second terminal and the gate being connected with each other; and a second transistor for allowing a current corresponding to the voltage of the gate of the second transistor to flow between a first terminal and a second terminal of the second transistor, the first terminal being connected to the other end of the second resistor, and the gate of the second transistor being connected to the gate of the first transistor. The current flowing in the first transistor is converted into the non-linear current flowing in the second transistor. According to the present invention, the circuit configuration can be simplified, and also, smooth, non-linear characteristics can be obtained.

For the first and second resistors, it is sufficient that the resistances thereof are different, and accordingly, it is sufficient that the line width or the line length thereof is different. If the resistance of the first resistor is not zero, the resistance of the second resistor may be zero.

[0007]

Another current generating circuit of the present invention includes: a first resistor and a second resistor, one end of each of the first resistor and the second resistor being connected to a power supply terminal to which a power supply voltage is supplied, the resistance of the first resistor and the resistance of the second resistor being different, and at least one of the first resistor and the second resistor being a variable resistor; a first transistor for allowing a current corresponding to the voltage of the gate of the first transistor to flow between a first terminal and a second terminal of the first transistor, the first terminal being connected to the other end of the first resistor, and the second terminal and the gate being connected with each other; and a second transistor for allowing a current corresponding to the voltage of the gate of the second transistor to flow between a first terminal and a second terminal of the second transistor, the first terminal being connected to the other end of the second resistor, and the gate of the second transistor being connected to the gate of the first transistor. According to the present invention, the circuit configuration can be simplified, and also, smooth, non-linear characteristics can be obtained.

Between the first resistor and the second resistor, only the first resistor may preferably be a variable

resistor. With this arrangement, the non-linear characteristics can be adjusted.

The variable resistor may preferably be configured such that a plurality of resistor devices having predetermined resistances are connected in series with each other or in parallel with each other.

[0008]

The above-described current generating circuits may be dependently connected, and the current flowing in the second transistor of the current generating circuit disposed at the first stage may be allowed to flow in the first transistor of the current generating circuit disposed at the second stage.

The current generating circuit may further include a D/A conversion circuit for converting digital data into a current signal indicating a current corresponding to the digital data and for allowing the current signal to flow in the first transistor.

[0009]

In order to achieve the above-described object, an electro-optical apparatus of the present invention includes: pixel circuits disposed at the intersections of a plurality of scanning lines and a plurality of data lines; a scanning-line drive circuit for selecting the scanning lines; and a data-line drive circuit including the current generating

circuit set forth in any one of claims 1 to 4, and supplying the current flowing in the second transistor of the current generating circuit to the data lines. The pixel circuit disposed at the intersection between one scanning line and one data line includes: a capacitor device for storing electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and an electro-optical device in which a current corresponding to the electrical charge stored in the capacitor device flows when the selection of the scanning line is finished. According to the present invention, the circuit configuration for obtaining non-linear characteristics can be simplified, and also, smooth, non-linear characteristics can be obtained.

This electro-optical apparatus may preferably include a setting circuit for setting the resistance of the first resistor or the second resistor of the current generating circuit to a desired value.

[0010]

Another electro-optical apparatus of the present invention includes: a plurality of types of pixel circuits corresponding to a plurality of primary colors, the pixel circuits corresponding to the same primary color being disposed at the intersections of a plurality of scanning lines and a plurality of data lines such that the pixel

circuits share the same data line; a scanning-line drive circuit for selecting the scanning lines; and a data-line drive circuit including the current generating circuit set forth in claim 3 for each of the primary colors, and supplying the current flowing in the second transistor of the current generating circuit corresponding to one primary color to the data line corresponding to the primary color. The pixel circuit disposed at the intersection between one scanning line and one data line includes: a capacitor device for storing electrical charge in accordance with the current flowing in the data line when the scanning line is selected by the scanning-line drive circuit; and an electro-optical device in which a current corresponding to the electrical charge stored in the capacitor device flows when the selection of the scanning line is finished. According to the present invention, the circuit configuration for obtaining non-linear characteristics can be simplified, and also, smooth, non-linear characteristics can be obtained.

This electro-optical apparatus may preferably include a setting circuit for setting the resistance of the first resistor or the second resistor of the current generating circuit for each of the primary colors. With this arrangement, adjustments to the non-linear characteristics can be simultaneously made for each of the primary colors.

When such a setting circuit is provided, a designation

circuit for designating the resistance to be set by the setting circuit may also be provided. The designation circuit may designate the resistance according to the detected temperature, or may read and designate the resistance from prestored resistances according to the display mode.

[0011]

The electro-optical apparatus may further include: a memory for storing digital data defining the grayscale of the electro-optical device; a control circuit for reading the digital data from the memory; and a D/A conversion circuit for converting the digital data read by the control circuit into a current signal indicating a current corresponding to the digital data, and for allowing the current signal to flow in the first transistor of the current generating circuit.

The electro-optical device of the electro-optical apparatus may preferably be an organic electro luminescence device.

An electronic unit of the present invention may preferably include the above-described electro-optical apparatus.

[0012]

[Description of the Embodiments]

An embodiment of the present invention is described

below with reference to the drawings. Fig. 1 illustrates the configuration of a current generating circuit according to an embodiment.

As shown in Fig. 1, a current generating circuit 10 includes a D/A conversion circuit 20 for receiving digital data Dpix that linearly defines the grayscale of pixels so as to generate a current signal exhibiting linear characteristics for the digital data Dpix, and also includes a non-linear characteristic generating circuit 40 for converting this current signal into a current signal exhibiting non-linear characteristics and outputting this current signal.

For the sake of description, it is now assumed that the digital data Dpix has 6 bits and defines the grayscale in 64 levels (two to the power of six) from "0" to "63" in decimal notation.

In this embodiment, the current generating circuit 10 is a combination of the D/A conversion circuit 20 and the non-linear characteristic generating circuit 40. Only the non-linear characteristic generating circuit 40 is, however, sometimes referred to as a current generating circuit (in a narrow sense).

[0013]

In the current generating circuit 10, reference is first made to the D/A conversion circuit 20. Fig. 2 is a

circuit diagram illustrating the configuration of the D/A conversion circuit 20.

In Fig. 2, a switch Sw0 is turned ON when the lowest bit D0 of the digital data Dpix is '1' and is turned OFF when the digital data Dpix is '0'. Similarly, switches Sw1 through Sw5 are turned ON when the fifth bit D1, the fourth bit D2, the third bit D3, the second bit D4, and the highest bit D5 of the digital data Dpix are '1', respectively, and are turned OFF when the corresponding bits are '0'.

One end of each of the switches Sw0 through Sw5 is connected to a common terminal N1, and the other end of the switch Sw0 is connected to the drain (electrode) of a transistor 30. Similarly, the other ends of the switches Sw1 through Sw5 are connected to the drains of transistors 31 through 35, respectively. The sources (electrodes) of the transistors 30 through 35 are grounded, i.e., they are connected to a common terminal to which the low-potential voltage of a power supply voltage is supplied.

[0014]

A common reference voltage Vref is applied between the gates and the sources of the transistors 30 through 35. Accordingly, when each transistor is operated in a saturation area, the current flowing between the source and the drain of the transistor is determined by a gain coefficient (current amplification factor) β. When the

ratio of the gain coefficient β of the transistors 30 through 35 is set to be 1:2:4:8:16:32, respectively, the current Iin flowing in the terminal N1 becomes the sum of the currents flowing in the transistors 30 through 35, and thus exhibits the characteristic shown in Fig. 3.

That is, the current Iin takes 0 when the digital data Dpix is minimum "0" (decimal notation), and linearly (strictly speaking, discretely) increases until Imax when the digital data Dpix increases to the maximum value "63".

[0015]

The non-linear characteristic generating circuit 40 is now described. Fig. 4 is a circuit diagram illustrating the configuration of the non-linear characteristic generating circuit 40. As shown in Fig. 4, the non-linear characteristic generating circuit 40 includes resistors 41 and 42 and p-channel transistors 51 and 52, and forms a current mirror circuit for converting the linear current Iin(I_1) flowing in the terminal N1 into a non-linear current Iout(I_2) so as to supply the non-linear current Iout to a terminal N2.

One end of the resistor 41 and one end of the resistor 42 are connected to a common terminal Nd to which the high-potential voltage V_{DD} of the power supply source is supplied. The source of the transistor 51 is connected to the other end of the resistor 41, and the gate and the drain of the

transistor 51 are connected with each other in a saturating manner. The source of the transistor 52 is connected to the other end of the resistor 42, the gate thereof is connected to the gate of the transistor 51, which is connected to the drain thereof in a saturating manner, and the drain of the transistor 52 is connected to the terminal N2.

Although the transistors 30 through 35, 51, and 52 assume FETs in this embodiment, they may be bipolar transistors and are not restricted to a particular type.

[0016]

It is now assumed that the voltage of the source of the transistor 51 (the other end of the resistor 41) is V_1, the source of the transistor 52 (the other end of the resistor 42) is V_2, the voltage of the gate of the transistor 52 (the gate of the transistor 51) is V_3, the gain coefficient of the transistor 51 is β_1, the gain coefficient of the transistor 52 is β_2, the threshold voltage of the transistors 51 and 52 is V_{th}, the resistance of the resistor 41 is R_1, and the resistance of the resistor 42 is R_2. In this case, if the current flowing in the transistor operating in the saturation area is determined by the square law of the gate-source voltage, the currents I_1 and I_2 can be expressed by equations (1) and (2), respectively.

$$I_1 = \{\beta_1(V_1-V_3-V_{th})^2\}/2 \quad \ldots (1)$$

$$I_2 = \{\beta_2(V_2-V_3-V_{th})^2\}/2 \quad \ldots (2)$$

[0017]

The voltage drops of the resistors 41 and 42 can be expressed by equations (3) and (4), respectively.

$$I_1 \cdot R_1 = V_{DD}-V_1 \quad \ldots (3)$$

$$I_2 \cdot R_2 = V_{DD}-V_2 \quad \ldots (4)$$

[0018]

Equation (1) can be modified as follows.

$$(2I_1/\beta_1)^{1/2} = V_1-V_3-V_{th} \quad \ldots (5)$$

By eliminating the term V_{DD} by using equations (3) and (4) and by solving equations (3) and (4) with respect to V_1, equation (6) can be determined.

$$V_1 = V_2-I_1 \cdot R_1+I_2 \cdot R_2 \quad \ldots (6)$$

Then, by substituting V_1 expressed in equation (6) into V_1 at the right side of equation (5), equation (7) can be determined, as shown in Fig. 6. Then, when the left side of equation (7) is substituted into the term within the parenthesis at the right side of equation (2), and then, the resulting equation is rearranged, as shown in Fig. 7, equation (8) is obtained.

Equation (8) is solved with respect to I_2, resulting in equation (9) shown in Fig. 8.

[0019]

In Fig. 4, for differentiating the resistors 41 and 42, it is sufficient that the resistances thereof are different, and accordingly, it is sufficient that the line width or the

line length of the resistors 41 and 42 is different. If the resistance of the resistor 41 is not zero, the resistance of the resistor 42 may be zero.

Then, for simplifying the characteristic indicated by equation (9), the terminal Nd and the source of the transistor 52 is short-circuited so that the resistance R_2 of the resistor 42 becomes zero. Then, equation (9) is simplified into equation (10) shown in Fig. 9.

In equation (10), the output current I_2 is expressed by a square function of the input current I_1, and thus, the characteristic of the output current I_2 in relation with the digital data Dpix can be indicated by sign a of Fig. 5. In Fig. 5, the output current I_2 is normalized as the relative current Iout in such a manner that it is 0% when the digital data Dpix is minimum "0" and it is 100% when the digital data Dpix is maximum "63".

As described above, according to this embodiment, the characteristic a of the output current I_2 (Iout) can be smooth, non-linear with respect to the digital data Dpix. The characteristic a can be approximated to a characteristic b (γ coefficient 2.2) which is considered to be ideal in an electro-optical apparatus described below.

[0020]

In equation (10) in Fig. 9, since the resistance R_1 of the resistor 41 is a coefficient of the input current I_1,

the rate by which the output current I_2 changes can be adjusted if the resistor 41 is a variable resistor. When the resistor 41 is set to be a variable resistor, for example, as shown in Fig. 10(a), instead of the resistor 41, an electronic volume consisting of a plurality of series-connected resistors and switches for turning ON or OFF across the corresponding resistors according to the bits of digital data Ds may be used. Alternatively, as shown in Fig. 10(b), an electronic volume consisting of a plurality of parallel-connected resistors and switches for turning ON or OFF the connections of the corresponding resistors according to the bits of the digital data Ds may be used. By using such an electronic volume, the resistance R_1 as the combined resistance in accordance with the digital data Ds can be set from outside the current generating circuit 10, thereby making it possible to adjust the rate by which the output current I_2 changes.

[0021]

Alternatively, as shown in Fig. 11, two or more current mirror circuits may be cascade-connected to form the non-linear characteristic generating circuit 40.

In Fig. 11, one end of a resistor 43 is grounded, and the other end thereof is connected to the source of an n-channel transistor 53 whose drain and gate are connected with each other in a saturating manner. The drain of the

transistor 53 is connected to the drain of the transistor 52. The source of an n-channel transistor 54 is grounded, the drain thereof is connected to the terminal N2, and the gate thereof is connected to the gate (drain) of the transistor 53.

With this configuration, the output current I_2 is indicated by a square function of the input current I_1, and a current I_3 flowing in the transistor 54 via the terminal N2 is indicated by a square function of the current I_2. This means that the current I_3 is indicated by a biquadrate function of the input current I_1. Accordingly, the characteristic of the current I_3 (Iout) for the digital data Dpix is indicated by sign c of Fig. 5, in which the level of γ correction can be increased compared to that of the characteristic indicated by sign a.

[0022]

A description is now given of an electro-optical apparatus using the above-described current generating circuit 10. Fig. 12 is a block diagram illustrating the configuration of the electro-optical apparatus.

As shown in Fig. 12, the electro-optical apparatus 100 includes a display panel 120 in which m scanning lines 102 and n data lines 104 intersect with each other (they are electrically insulated from each other), a pixel circuit 110 being provided at each intersection of the scanning lines

102 and the data lines 104. The electro-optical apparatus 100 also includes a scanning-line drive circuit 130 for driving the individual scanning lines 102, a data-line drive circuit 140 for driving the individual data lines 104, a memory 150 for storing digital data Dmem, supplied from an external device, for example, a computer, defining the grayscale level of each pixel forming an image to be displayed, a control circuit 160 for controlling all the elements, and a power supply circuit 170 for supplying power to all the elements.

In the electro-optical apparatus 100, too, it is assumed that the digital data Dpix has 6 bits and defines the grayscale level of each pixel in 64 levels (two to the power of six) by one of "0" to "63" in decimal notation.

[0023]

The scanning-line drive circuit 130 generates scanning signals Y1, Y2, Y3, ..., Ym used for sequentially selecting the scanning lines 102 one by one. More specifically, as shown in Fig. 13, the scanning-line drive circuit 130 supplies a pulse having a width corresponding to one horizontal scanning period (1H) to the first scanning line 102 as the scanning signal Y1 from the start of one vertical scanning period (1F), and then sequentially shifts this pulse to supply the scanning signals Y2, Y3, ..., Ym to the second, third, ..., m-th scanning lines 102, respectively.

Generally, when the scanning signal Yi supplied to the i-th scanning line 102 (i is an integer satisfying $1 \leq i \leq m$) becomes H level, it means that the i-th scanning line 102 has been selected.

In addition to the scanning signals Y1, Y2, Y3, ..., Ym, the scanning-line drive circuit 130 also generates signals having logical levels inverted from those of the scanning lines Y1, Y2, Y3, ..., Ym as light-emission control signals Vg1, Vg2, Vg3, ..., Vgm, and supplies them to the display panel 120. Signal lines through which the light-emission control signals are supplied are not shown in Fig. 12.

[0024]

The control circuit 160 controls the scanning-line drive circuit 130 to select the scanning lines 102. Also, in synchronization with the selection of the scanning lines 102, the control circuit 160 reads the digital data Dpix-1 through Dpix-n corresponding to the first through n-th data lines 104 from the memory 150 and supplies them to the data-line drive circuit 140.

As shown in Fig. 14, the data-line drive circuit 140 has the current generating circuit 10, which is the feature of this invention, for each data line 104. Generally, digital data Dpix-j corresponding to the intersection of the selected scanning line 102 and the j-th data line 104 (j is

an integer satisfying $1 \leq j \leq n$) is supplied to the j-th current generating circuit 10. In this electro-optical apparatus 100, the j-th current generating circuit 10 is, for example, a combination of the D/A conversion circuit 20 shown in Fig. 2 and the non-linear characteristic generating circuit 40 shown in Fig. 11, and generates the non-linear current Iout for the supplied digital data Dpix-j and allows the current Iout to flow in the j-th data line 104. For example, the third current generating circuit 10 generates the current Iout corresponding to the value of the digital data Dpix-3 at the intersection of the selected scanning line 102 and the third data line 104, and allows the current Iout to flow in the third data line 104.

[0025]

Various modes can be considered to implement the commercial availability of the electro-optical apparatus 100. For example, the elements 120, 130, 140, 150, 160, and 170 of the electro-optical apparatus 100 may be formed of independent components, or part of or all of the elements may be integrally formed (for example, the scanning-line drive circuit 130 and the data-line drive circuit 140 may be integrally formed, or part of or all of the elements except for the display panel 120 may be formed as a programmable IC chip, and the functions of the elements are implemented by a software program written into the IC chip).

[0026]

The pixel circuits 110 of the electro-optical apparatus 100 are as follows. Fig. 15 is a circuit diagram illustrating an example of the configuration of the pixel circuit 110. The structures of all the pixel circuits 110 are the same, and to describe the pixel circuit 110 by generalizing the scanning lines, the pixel circuit 110 provided at the intersection of the i-th scanning line 102 and a certain data line 104 is now discussed.

As shown in Fig. 15, the pixel circuit 110 provided at the intersection of the scanning line 102 and the data line 104 includes four thin film transistors (hereinafter simply referred to as "TFTs") 1102, 1104, 1106, and 1108, a capacitor device 1120, and an organic EL device 1130.

The source of the p-channel TFT 1102 is connected to a power supply line 109 to which a high-potential voltage Vdd of the power supply source is applied, and the drain thereof is connected to the drain of the n-channel TFT 1104, the drain of the n-channel TFT 1106, and the source of the n-channel TFT 1108.

[0027]

One end of the capacitor device 1120 is connected to the power supply line 109 and the other end thereof is connected to the gate of the TFT 1102 and the drain of the TFT 1108. The gate of the TFT 1104 is connected to the

scanning line 102 and the source thereof is connected to the data line 104. The gate of the TFT 1108 is connected to the scanning line 102.

The gate of the TFT 1106 is connected to a light-emission control line 108, and the source thereof is connected to the anode of the organic EL device 1130. The light-emission control signal Vgi is supplied to the light-emission control line 108 by the scanning-line drive circuit 130. In the organic EL device 1130, an organic EL layer is disposed between the anode and the cathode so that light is emitted with a luminance level in accordance with the forward current. The cathodes of the organic EL devices 1130 in all the pixel circuits 110 are a common electrode, and are grounded to a low potential (reference potential) of the power supply source.

[0028]

With this configuration, when the i-th scanning line 102 is selected so that the scanning signal Yi becomes H level, the n-channel TFT 1108 is conducted (ON) across the source and the drain, and thus, the TFT 1102 serves as a diode whose gate and drain are connected to each other. When the scanning signal Yi supplied to the scanning line 102 becomes H level, the n-channel TFT 1104 is also conducted as in the TFT 1108. Thus, the current Iout generated from the current generating circuit 10 flows in

the order of the power supply line 109, the TFT 1102, the TFT 1104, and the data line 104, and also, the electrical charge in accordance with the gate potential of the TFT 1102 is stored in the capacitor device 1120.

[0029]

Subsequently, when the selection of the i-th scanning line 102 is completed so that the scanning signal Yi becomes L level, the TFTs 1104 and 1108 become non-conducted (OFF). However, since the storage state of the electrical charge in the capacitor device 1120 does not change, the gate of the TFT 1102 is maintained at the voltage when the current Iout has flown.

When the scanning signal Yi becomes L level, the light-emission control signal Vgi becomes H level. Accordingly, the n-channel TFT 1106 is turned ON so that a current flows across the source and the drain of the TFT 1102 in accordance with the gate voltage. More specifically, this current flows in the order of the power supply line 109, the TFT 1102, the TFT 1106, and the organic EL device 1130. Thus, the organic EL device 1130 emits light with a luminance level in accordance with the current.

[0030]

The current flowing in the organic EL device 1130 is determined by the gate voltage of the TFT 1102, and this gate voltage is the voltage maintained in the capacitor

device 1120 when the current Iout has flown in the data line 104 by the H-level scanning signal. Accordingly, the current flowing in the organic EL device 1130 when the light-emission control signal Vgi becomes H level is substantially equal to the previous current Iout.

Thus, even if there is a variation in the characteristics of the TFTs 1102 in the overall pixel circuits 110, the current having the same level can be supplied to the organic EL devices 1130 of the pixel circuits 110, thereby preventing a display image from being non-uniform, which would be caused by the above-described characteristic variation.

[0031]

Only one pixel circuit 110 has been described. However, since the i-th scanning line 102 is shared by the m pixel circuits 110, an operation similar to the above-described operation is performed in the m pixel circuits 110 when the scanning line Yi becomes H level.

The scanning signals Y1, Y2, Y3, ..., Ym become H level exclusively, as shown in Fig. 13. Thus, in each pixel circuit 110, the gate voltage of the TFT 1102 is maintained at the voltage stored in the capacitor device 1120 when the current Iout flows in accordance with the grayscale level of the organic EL device 1130.

[0032]

The channel types of TFTs 1102, 1104, 1106, and 1108 are not restricted to the types described above, and p-channel and n-channel TFTs may be suitably selected.

The reason for using the current generating circuit 10 shown in Fig. 11 in the data-line drive circuit 140 is as follows. Since, in the pixel circuit 110, the organic EL device 1130 is driven by the p-channel TFT 1102, a current must flow in the organic EL device 1130 by withdrawing a current from the pixel circuit 110 via the data line 104.

Accordingly, if the pixel circuit 110 is configured such that the organic EL device 1130 is driven by the n-channel TFT 1102, the current generating circuit 10 shown in Fig. 4 or 11 can be used so that a current flows in the organic EL device 1130 by being supplied to the pixel circuit 110 via the data line 104.

In the electro-optical apparatus 100, the light-emission control signals Vg1, Vg2, Vg3, ..., Vgm are supplied by the scanning-signal drive circuit 130 by inverting the logical levels of the scanning lines Y1, Y2, Y3, ..., Ym. However, the light-emission control signals Vg1, Vg2, Vg3, ..., Vgm may be supplied by a separate circuit, or the periods during which the light-emission control signals Vg1, Vg2, Vg3, ..., Vgm become an active level (H level) may be decreased.

[0033]

When performing color display in an electro-optical apparatus, a typical configuration of the electro-optical apparatus is as follows. Three pixel circuits correspond to the three primary colors, such as R (red), G (green), and B (blue) so that they form one pixel of a display image. With this configuration, to adjust the color balance, R, G, and B organic EL devices must adjust the γ characteristics for the individual primary colors. It is sometimes necessary for electro-optical apparatuses to adjust and set the γ characteristics later according to the environments (the intensity of extraneous light, temperature, etc.), the signal format, or the display mode.

[0034]

An electro-optical apparatus that satisfies such requirements is described below. Fig. 16 illustrates the arrangement of R, G, and B pixel circuits in the display panel 120 of this electro-optical apparatus. As shown in Fig. 16, the R, G, and B pixel circuits 110 are arranged in the form of a stripe in which the same color is disposed in one column (in the direction in which the data lines 104 are extended), and the pixel circuits 110 having the same color arranged in the same column share the same data line 104.

Fig. 17 illustrates the configuration of the data-line drive circuit 140 of this electro-optical apparatus. The data-line drive circuit 140 is similar to the configuration

shown in Fig. 14 in that the current generating circuit 10 is provided for each data line 104. However, since the data lines 104 correspond to R, G, and B, the current generating circuits 10 are also associated with R, G, and B. In these current generating circuits 10, the resistor 41 of the non-linear characteristic generating circuit 40 is a variable resistor, and the resistance thereof is set by an electronic volume, such as that shown in Fig. 10(a) or 10(b).

[0035]

A designation circuit 1410 is a temperature sensor for detecting the temperature, an optical sensor for detecting the intensity of extraneous light, a determination circuit for determining the format of an image signal, or a switch for designating a display mode, and supplies information Q indicating a detection result, a determination result, or a designation result, to a setting circuit 1420.

The setting circuit 1420 generates digital data Ds according to the individual colors based on the information Q, and supplies the digital data Ds to the current generating circuits 10 of the corresponding colors. The digital data Ds can be generated from the information Q according to various techniques. For example, the digital data Ds can be computed by using a function using the information Q as an argument, or the information Q can be converted into the digital data Ds by using a preset table.

In the electro-optical apparatus constructed as described above, the non-linear characteristics of the current generating circuit 10 can be suitably adjusted for each of R, G, and B according to the environment, the mode, etc.

If adjustments of the non-linear characteristics according to the environment, mode, etc. are not required for each of R, G, and B, the same digital data Ds can be used, as shown in Fig. 18. In this case, the circuit can be simplified compared to the configuration shown in Fig. 17.

[0036]

Although the data-line drive circuit 140 shown in Fig. 14 or 17 has the current generating circuit 10 for each data line 104, it may be configured, such as that shown in Fig. 19. That is, in this configuration, a shift register 1430 sequentially selects the data lines 104 one by one during one horizontal period, and also, a current generated by the current generating circuit 10 flows in the selected data line 104 (dot-sequential system).

In the configuration of this dot-sequential system, too, color display may be performed, and the designation circuit 1410 and the setting circuit 1420 shown in Fig. 17 may be provided.

[0037]

In the electro-optical apparatus 100 described above,

the current generating circuit 10, which is the feature of the present invention, is used in the data-line drive circuit of an organic EL panel. However, the current generating circuit 10 may be used in various display panels other than the organic EL panels, for example, FED (Field Emission Display) panels.

[0038]

A description is now given of some examples of electronic units to which the electro-optical apparatus 100 is applied.

Fig. 20 is a perspective view illustrating the configuration of a mobile personal computer to which the electro-optical apparatus 100 is applied. In Fig. 20, a personal computer 2100 includes a main unit 2104 provided with a keyboard 2102 and the electro-optical apparatus 100, which serves as a display unit.

[0039]

Fig. 21 is a perspective view illustrating the configuration of a cellular telephone to which the above-described electro-optical apparatus 100 is applied. In Fig. 21, a cellular telephone 2200 includes a plurality of operation buttons 2202, an earpiece 2204, a mouthpiece 2206, and the above-described electro-optical apparatus 100.

[0040]

Fig. 22 is a perspective view illustrating the

configuration of a digital still camera having the above-described electro-optical apparatus 100 as a finder. In a silver-salt camera, a film is exposed to light by an optical image of a subject. In contrast, in a digital still camera 2300, an optical image of a subject is photo-electrically converted by an image-capturing device, for example, a CCD (Charge Coupled Device), so as to generate and store an image-captured signal. At the rear of a main unit 2302 of the digital still camera 2300, the above-described electro-optical apparatus 100 is disposed.

This electro-optical apparatus 100, which displays an image based on an image-captured signal, serves as a finder for displaying a subject. On the front surface (back surface in Fig. 22) of the main unit 2302, a light-receiving unit 2304 containing an optical lens, a CCD, etc., is provided.

[0041]

After checking the subject image displayed on the electro-optical apparatus 100, a photographer presses a button 2306, and then, a CCD image-captured signal is transferred to and stored in a memory of a circuit board 2308.

In this digital still camera 2300, video-signal output terminals 2312 for external display and an input/output terminal 2314 for data communication are provided at a side

surface of the case 2302.

[0042]

The electronic unit to which the electro-optical apparatus 100 is applied includes, not only the personal computer shown in Fig. 20, the cellular telephone shown in Fig. 21, and the digital still camera shown in Fig. 22, but also liquid crystal televisions, view-finder or monitor-direct-view-type display video cassette recorders, car navigation systems, pagers, digital diaries, calculators, word processors, workstations, videophones, POS terminals, devices provided with touch panels, etc. Of course, the above-described electro-optical apparatus 100 can be used as the display portion of these various electronic units.

[Brief Description of the Drawings]

[Fig. 1] Fig. 1 illustrates the configuration of a current generating circuit according to an embodiment of the present invention.

[Fig. 2] Fig. 2 illustrates the configuration of a D/A conversion circuit in the same current generating circuit.

[Fig. 3] Fig. 3 illustrates an input/output characteristic of the same D/A conversion circuit.

[Fig. 4] Fig. 4 illustrates the configuration of a non-linear characteristic generating circuit in the same current generating circuit.

[Fig. 5] Fig. 5 illustrates an input/output

characteristic of the same current generating circuit.

[Fig. 6] Fig. 6 illustrates an equation expressing the characteristic of the same current generating circuit.

[Fig. 7] Fig. 7 illustrates an equation expressing the characteristic of the same current generating circuit.

[Fig. 8] Fig. 8 illustrates an equation expressing the characteristic of the same current generating circuit.

[Fig. 9] Fig. 9 illustrates an equation expressing the characteristic of the same current generating circuit.

[Fig. 10] Fig. 10 illustrates examples of applications of the same current generating circuit.

[Fig. 11] Fig. 11 illustrates an example of applications of the same current generating circuit.

[Fig. 12] Fig. 12 illustrates an electro-optical apparatus to which the same current generating circuit is applied.

[Fig. 13] Fig. 13 illustrates the operation of a scanning-line drive circuit of the same electro-optical apparatus.

[Fig. 14] Fig. 14 illustrates a data-line drive circuit of the same electro-optical apparatus.

[Fig. 15] Fig. 15 illustrates a pixel circuit of the same electro-optical apparatus.

[Fig. 16] Fig. 16 illustrates the arrangement of the pixel circuits when color display is performed.

[Fig. 17] Fig. 17 illustrates an example of applications of the same data-line drive circuit.

[Fig. 18] Fig. 18 illustrates an example of applications of the same data-line drive circuit.

[Fig. 19] Fig. 19 illustrates an example of applications of the same data-line drive circuit.

[Fig. 20] Fig. 20 illustrates a personal computer using the same electro-optical apparatus.

[Fig. 21] Fig. 21 illustrates a cellular telephone using the same electro-optical apparatus.

[Fig. 22] Fig. 22 illustrates a digital still camera using the same electro-optical apparatus.

[Reference Numerals]

10 ... current generating circuit, 20 ... D/A conversion circuit, 40 ... non-linear characteristic generating circuit, 41 ... resistor (first resistor), 42 ... resistor (second resistor), 51 ... transistor (first transistor), 52 ... transistor (second transistor), 100 ... electro-optical apparatus, 102 ... scanning line, 104 ... data line, 110 ... pixel circuit, 120 ... display panel, 130 ... scanning-line drive circuit, 140 ... data-line drive circuit, 150 ... memory, 160 ... control circuit, 1120 ... capacitor device, 1130 ... organic EL device, 2100 ... personal computer, 2200 ... cellular telephone, 2300 ... digital still camera

[Name of Document] ABSTRACT

[Abstract]

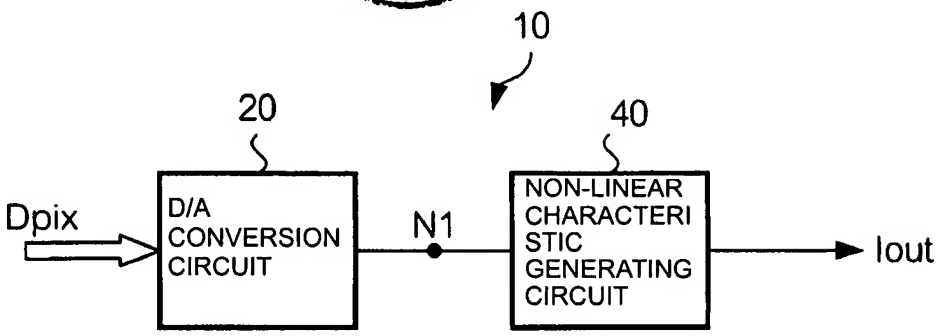
[Object] To form a simple circuit configuration and to convert a current I_1 to a current I_2 having smooth, non-linear characteristics.

[Solving Means] One end of each of resistors 41 and 42 whose resistances are different is connected to a power supply terminal Nd to which a power supply voltage V_{DD} is supplied. The source of a transistor 51 is connected to the other end of the resistor 41, and is also connected to the gate in a saturating manner. The source of a transistor 52 is connected to the other end of the resistor 42, and the gate of the transistor 52 is connected to the gate of the transistor 51, which is connected to the drain thereof in a saturating manner. A current I_2 flowing in the transistor 52 is a function equal to the square of a current I_1 flowing in the transistor 51, thereby exhibiting smooth, non-linear characteristics.

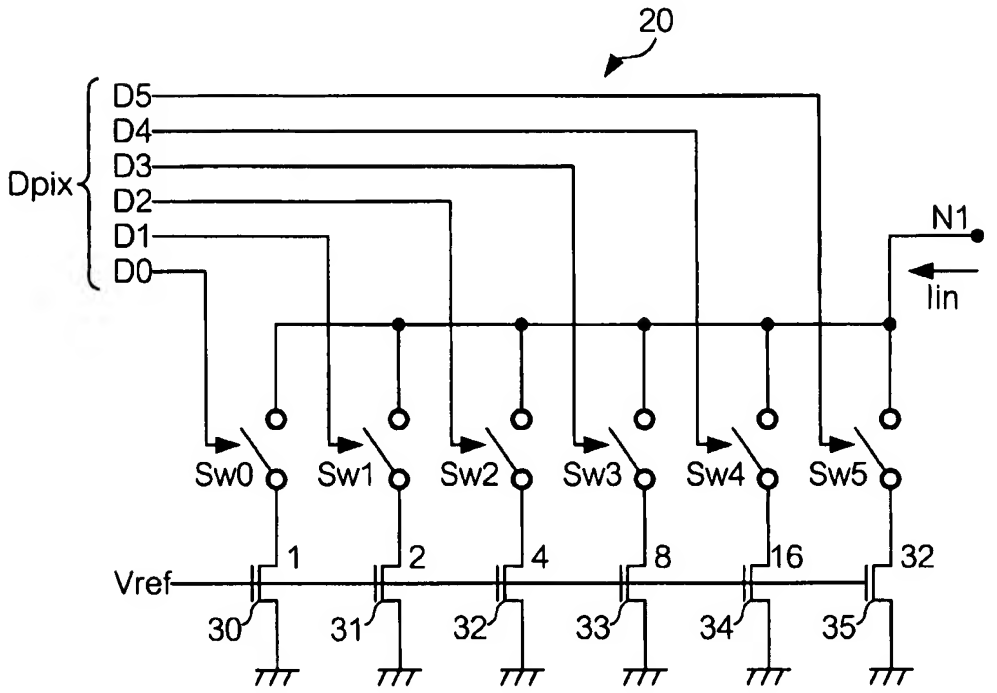
[Selected Figure] Fig. 4

[Name of Document] DRAWINGS

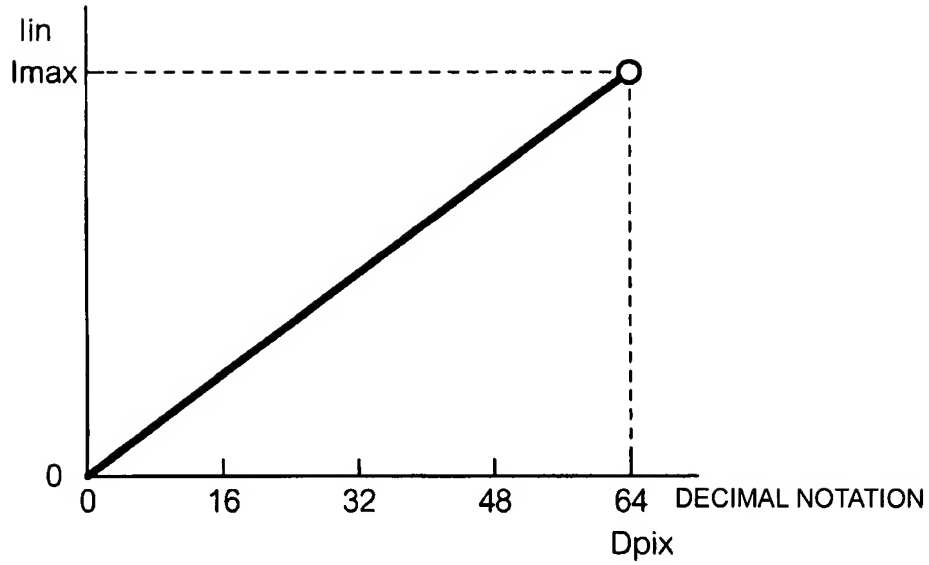
[FIG. 1]



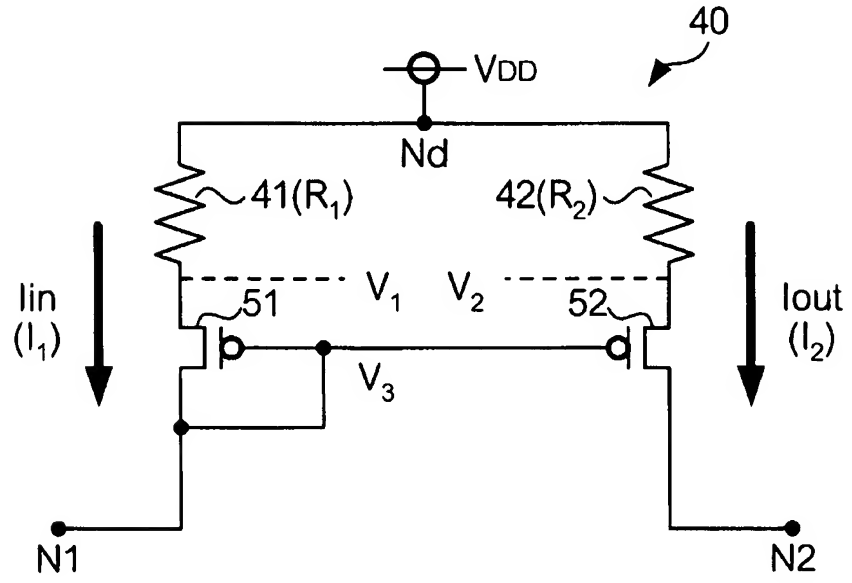
[FIG. 2]



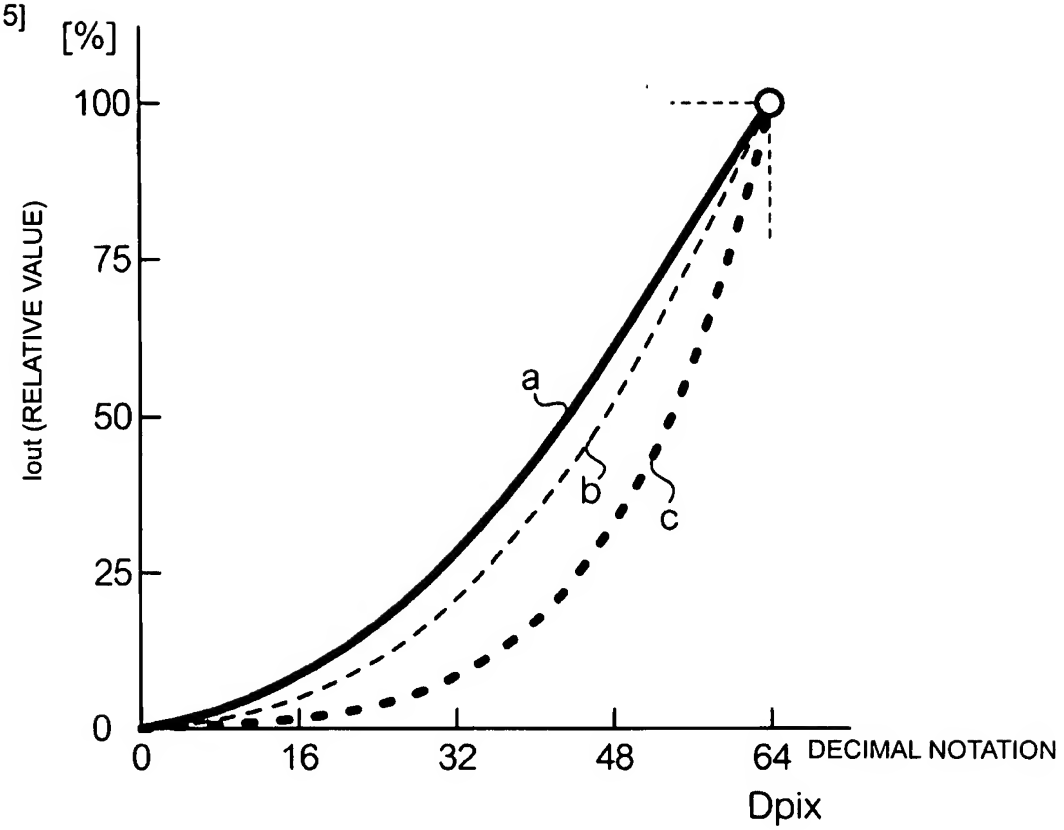
[FIG. 3]


Iin
Imax
0
0
16
32
48
64
DECIMAL NOTATION
Dpix

[FIG. 4]


40
VDD
Nd
41(R1)
42(R2)
Iin
(I1)
51
V1
V2
52
Iout
(I2)
V3
N1
N2

[FIG. 5]



[FIG. 6]

$$\sqrt{\frac{2I_1}{\beta_1}} = V_2 - I_1 \bullet R_1 + I_2 \bullet R_2 - V_3 - V_{th}$$

$$\therefore I_1 \bullet R_1 - I_2 \bullet R_2 + \sqrt{\frac{2I_1}{\beta_1}} = V_2 - V_3 - V_{th} \cdots\cdots (7)$$

[FIG. 7]

$$I_2 = \frac{1}{2}\beta_2\left(I_1 \bullet R_1 - I_2 \bullet R_2 + \sqrt{\frac{2I_1}{\beta_1}}\right)^2$$

$$\therefore \frac{2I_2}{\beta_2} = (I_1 \bullet R_1 - I_2 \bullet R_2)^2 + 2(I_1 \bullet R_1 - I_2 \bullet R_2)\sqrt{\frac{2I_1}{\beta_1}} + \frac{2I_1}{\beta_1}$$

$$= I_1^2 \bullet R_1^2 - 2I_1 \bullet R_1 \bullet I_2 \bullet R_2 + I_2^2 \bullet R_2^2 + 2I_1 \bullet R_1\sqrt{\frac{2I_1}{\beta_1}} - 2I_2 \bullet R_2\sqrt{\frac{2I_1}{\beta_1}} + \frac{2I_1}{\beta_1}$$

$$\therefore \quad R_2^2 \bullet I_2^2 - 2\left(\frac{1}{\beta_2} + I_1 \bullet R_1 \bullet R_2 + R_2\sqrt{\frac{2I_1}{\beta_1}}\right)I_2 + \left(\sqrt{\frac{2I_1}{\beta_1}} + I_1 \bullet R_1\right)^2 = 0 \cdots\cdots (8)$$

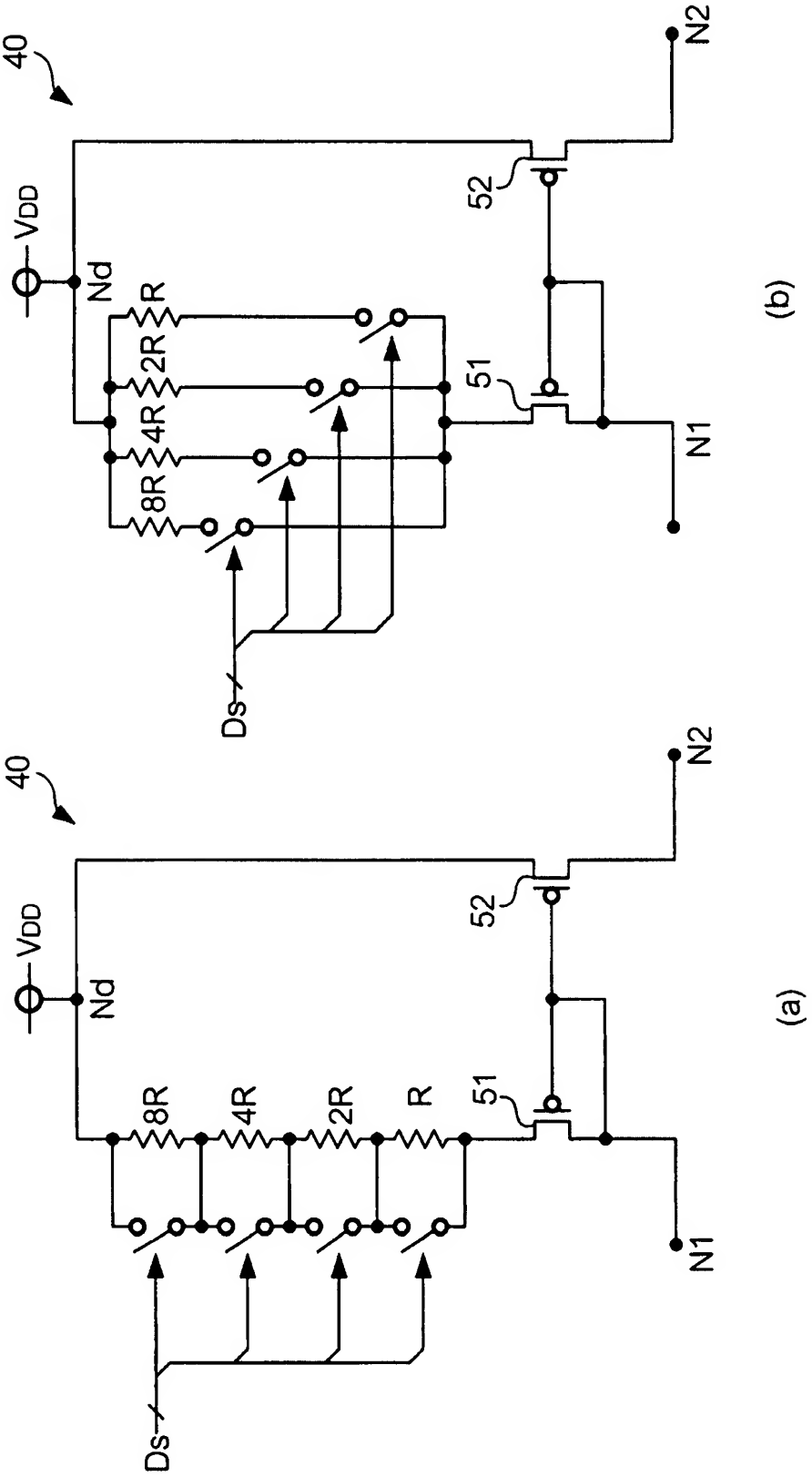
[FIG. 8]

$$I_2 = \frac{\frac{1}{\beta_2} + I_1 \bullet R_1 \bullet R_2 + R_2\sqrt{\frac{2I_1}{\beta_1}} + \sqrt{\left(\frac{1}{\beta_2} + I_1 \bullet R_1 \bullet R_2 + R_2\sqrt{\frac{2I_1}{\beta_1}}\right)^2 - R_2^2\left(\sqrt{\frac{2I_1}{\beta_1}} + I_1 \bullet R_1\right)^2}}{R_2^2} \cdots (9)$$

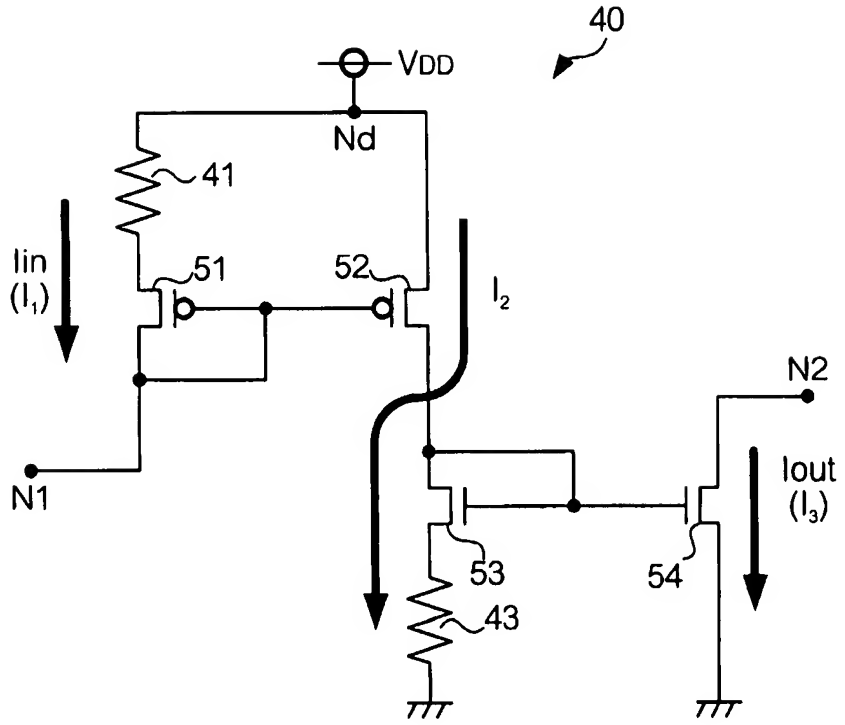
[FIG. 9]

$$I_2 = \frac{1}{2}\beta_2\left(\sqrt{\frac{2I_1}{\beta_1}} + I_1 \bullet R_1\right)^2 \cdots\cdots (10)$$

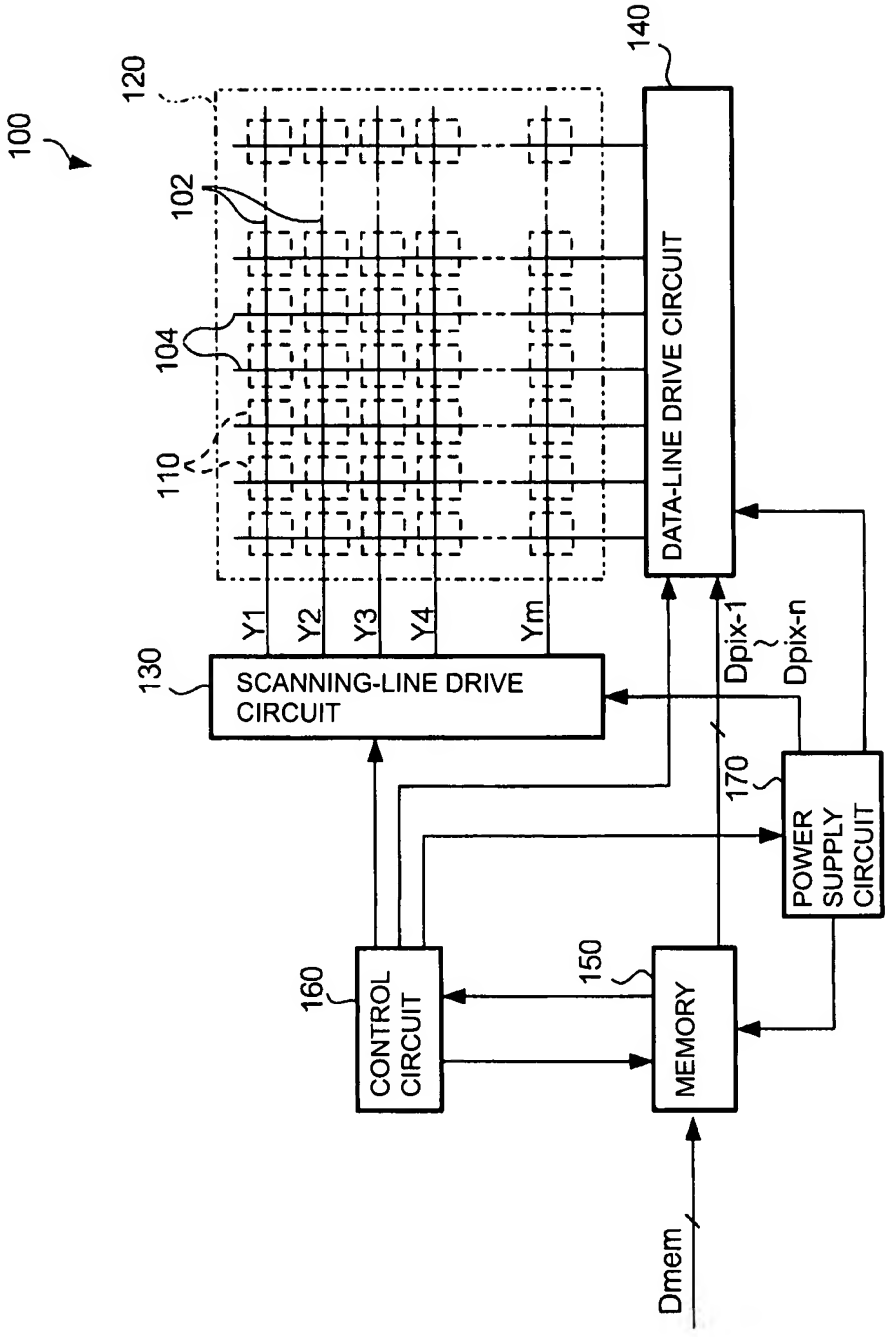
[FIG. 10]


40
VDD
Nd
R
2R
4R
8R
Ds
52
51
N2
N1
(b)
40
VDD
Nd
8R
4R
2R
R
Ds
52
51
N2
N1
(a)

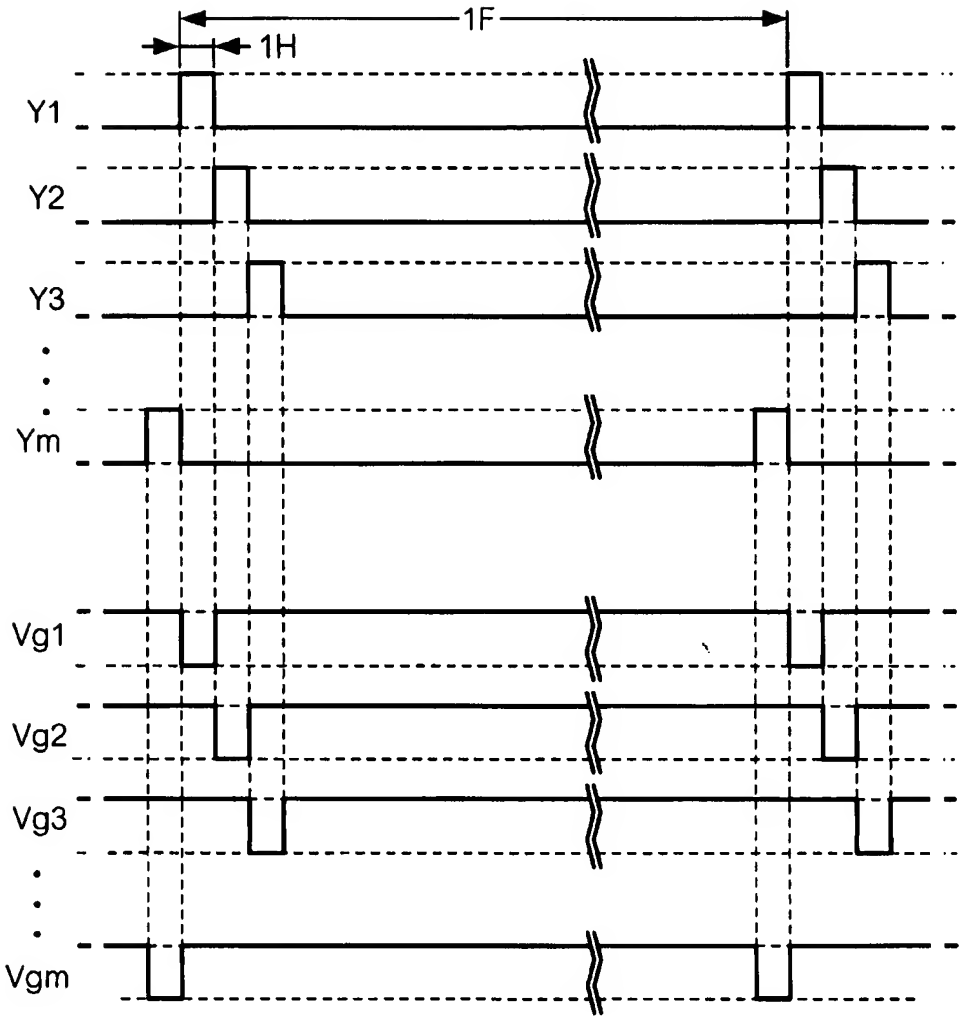
[FIG. 11]



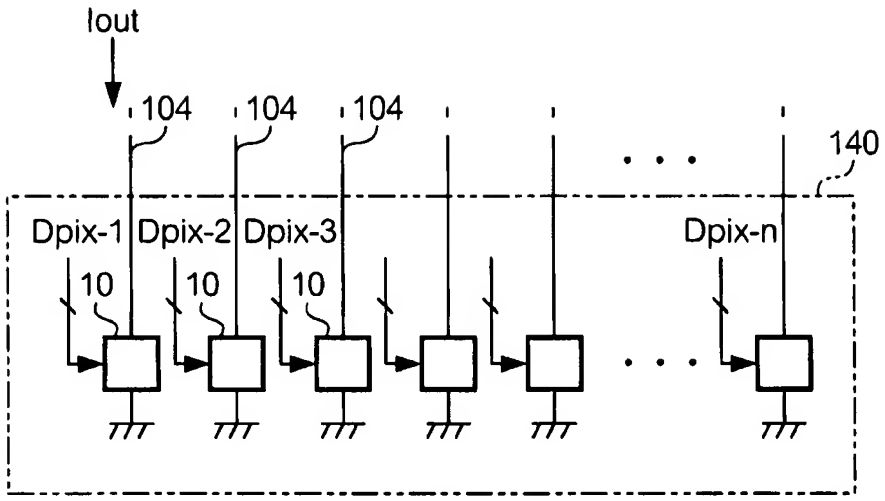
[FIG. 12]


100
120
140
102
104
110
DATA-LINE DRIVE CIRCUIT
Y1
Y2
Y3
Y4
Ym
130
SCANNING-LINE DRIVE CIRCUIT
Dpix-1
Dpix-n
170
POWER SUPPLY CIRCUIT
160
CONTROL CIRCUIT
150
MEMORY
Dmem

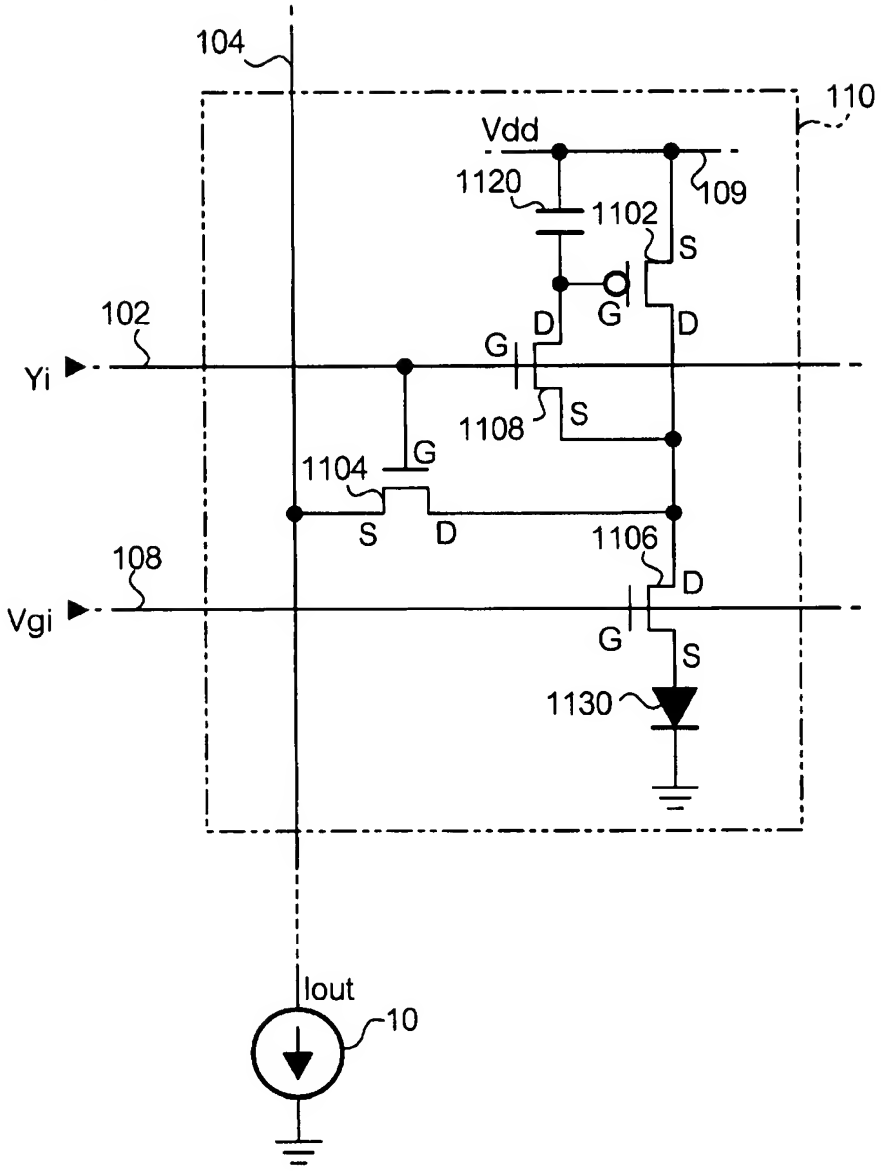
[FIG. 13]



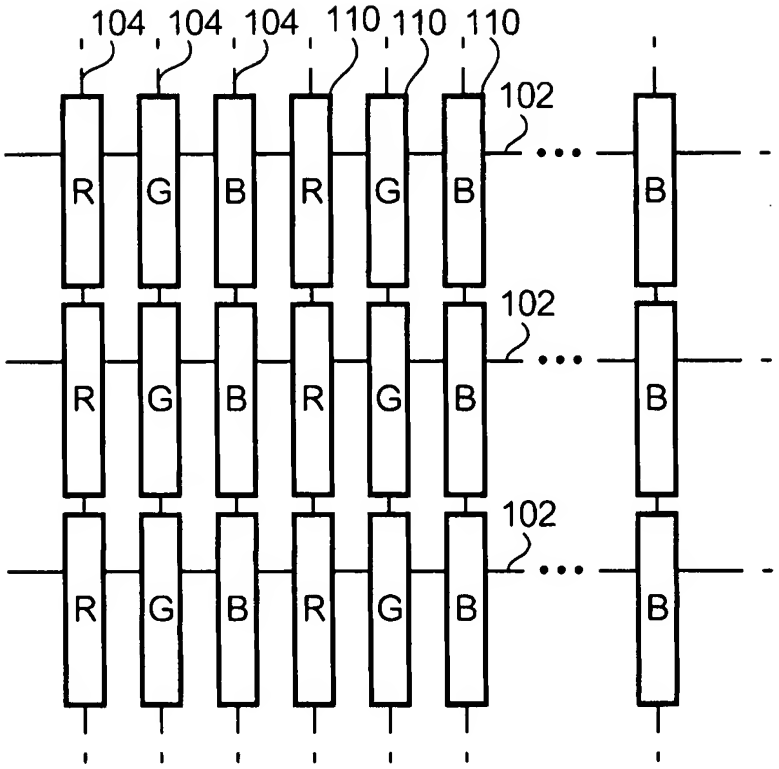
[FIG. 14]



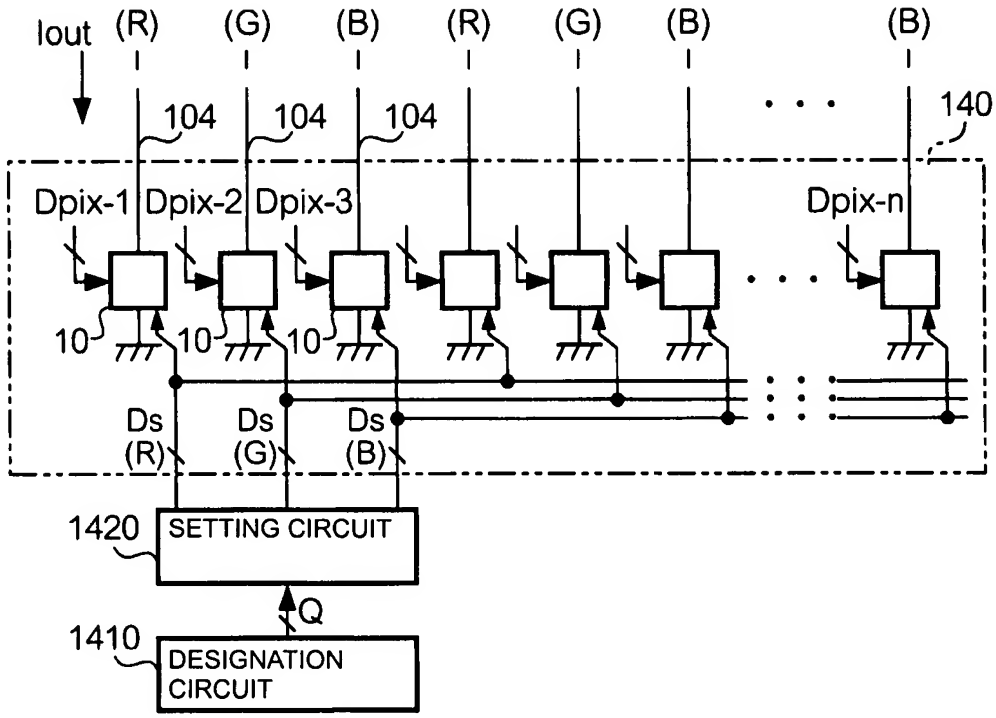
[FIG. 15]


104
110
Vdd
1120
1102
109
S
G
D
D
102
Yi
G
1108
S
1104
G
S
D
1106
D
108
Vgi
G
S
1130
Iout
10

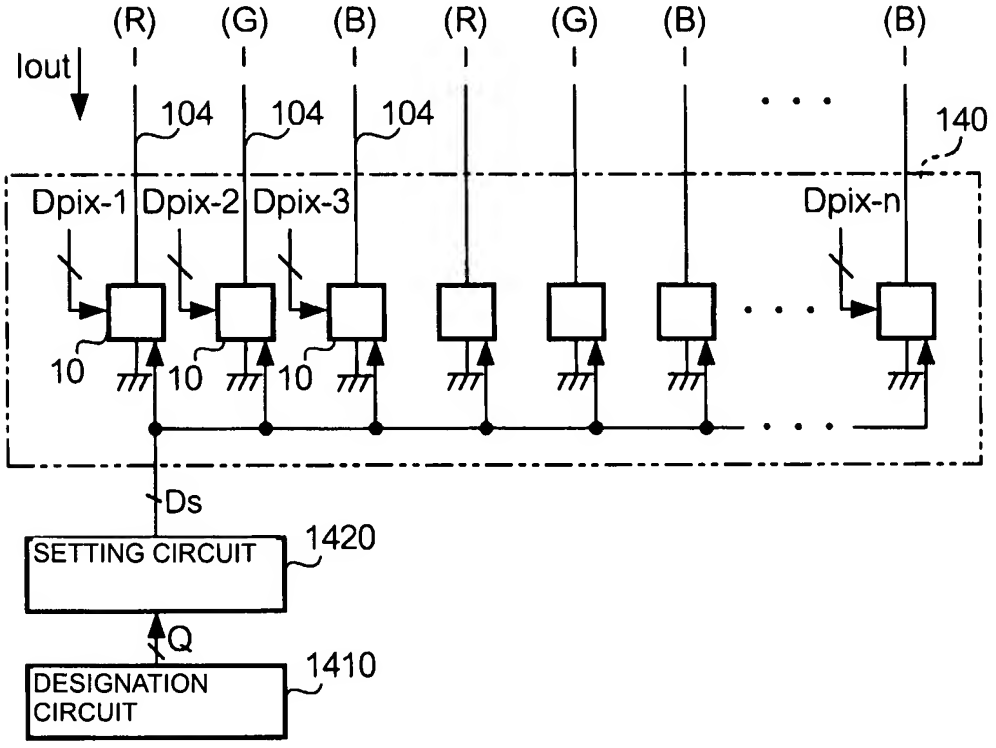
[FIG. 16]



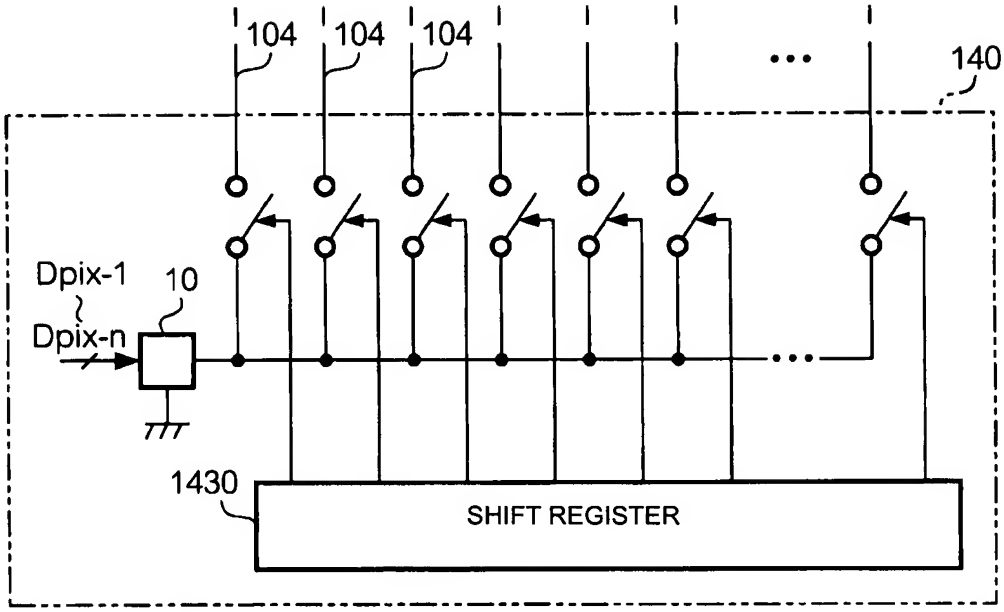
[FIG. 17]


Iout
(R)
(G)
(B)
(R)
(G)
(B)
(B)
104
104
104
140
Dpix-1
Dpix-2
Dpix-3
Dpix-n
10
10
10
Ds
(R)
Ds
(G)
Ds
(B)
1420
SETTING CIRCUIT
Q
1410
DESIGNATION CIRCUIT

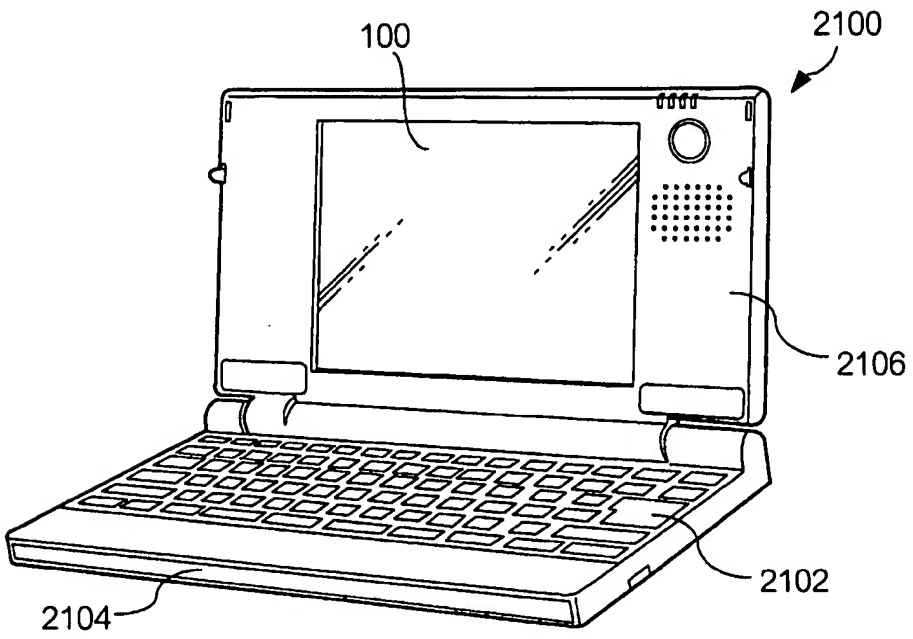
[FIG. 18]


(R)
(G)
(B)
(R)
(G)
(B)
(B)
Iout
104
104
104
140
Dpix-1
Dpix-2
Dpix-3
Dpix-n
10
10
10
Ds
SETTING CIRCUIT
1420
Q
DESIGNATION CIRCUIT
1410

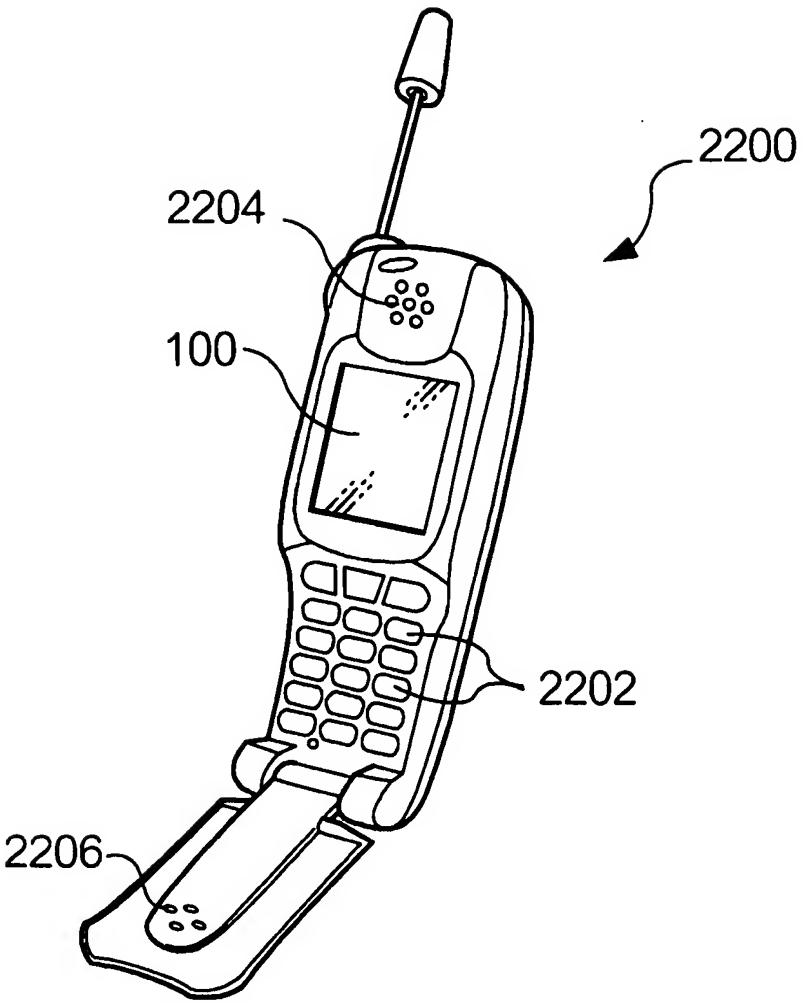
[FIG. 19]


104
104
104
140
Dpix-1
Dpix-n
10
1430
SHIFT REGISTER

[FIG. 20]


100
2100
2106
2102
2104

[FIG. 21]



[FIG. 22]